PATENT ABSTRACTS OF JAPAN

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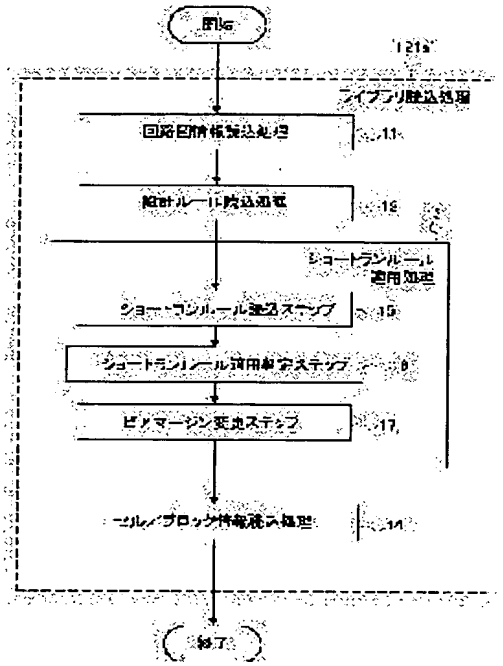
(54) WIRING METHOD FOR AUTOMATIC LOCATION WIRING SYSTEM AND RECORDING MEDIUM WITH RECORDED WIRING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To execute wiring while effectively utilizing short-run rules in an automatic location wiring system, which is not correspondent to the short-run rules.
SOLUTION: In a discrimination step 16 for short-run rule application, it is discriminated whether or not the short-run rules can be applied to the counter location spots of a via cell of the spot of a smallest wiring interval, and wiring or via cell. When the short-run rules can be applied in a via margin change step 17, via cell data are prepared at the time of wiring, in which a via margin is reduced so as to satisfy the minimum wiring interval with no short-run rule, automatic wiring processing is executed while using these data and in output processing of the wiring result, and the via cell data at the time of wiring are replaced with the artwork data of the via cell having the original via margin and outputted.



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PARTIAL TRANSLATION
<SPECIFICATION>

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[0022]
[Embodiments] (First Embodiment) An embodiment of the present invention will be described below in conjunction with drawings. Figure 1 briefly describes the flow of actions to be performed in a semiconductor design supporting system in accordance with the embodiment of the present invention by taking a gate array CAD system for instance. The flow described in Fig. 1 is implemented in a system similar to the one shown in Fig. 5.
[0023] Referring to Fig. 1, a reference numeral 14 denotes a hierarchical development block that flatly develops a circuit diagram 14a having a hierarchical structure and transmits a net list 19 by providing internal components such as macro functions and simulation models in the form of a library. The hierarchical development block 14 has the capability to change the names of cells, which share the same capability and are driven with different supply potentials, according to the supply potentials. Reference numeral 15 denotes a virtual wiring length-based logical simulation block that converts a virtual wiring length registered in a library 20 into a resistive or capacitive component so as to calculate a delay, and performs simulation on the basis of the result of the calculation. Reference numeral 16 denotes a layout block that arranges circuit elements, which are indicated in a circuit diagram, in the form of an LSI, and routes signals among the circuit elements. Reference numeral 17 denotes a real wiring length-based logical simulation block that converts a real wiring length, which is determined as a result of layout 16, into a resistive or capacitive component so as to calculate a delay, and performs simulation on the basis of the result of the calculation. Reference Numeral 18 denotes a test program

production block that produces a test program which checks a product using a test pattern, which the logical simulation blocks 15 and 17 use for simulation, to see if the product is acceptable or defective. Reference numeral 19 denotes a net list A produced by the hierarchical development block 14 according to the present embodiment. Reference numeral 20 denotes a library A required by the CAD system in accordance with the present embodiment.

[0024] The hierarchical development block 14, logical simulation block 15, layout block 16, logical simulation block 17, test product production block 18, library A 20 that are shown in Fig. 1 have fundamentally the same capabilities as the hierarchical development block 1, logical simulation block 2, layout block 3, logical simulation block 4, test program production block 5, and library 6 respectively that are shown in Fig. 6. However, the system shown in Fig. 1 has the library and net list modified so that they can specify which of circuit elements is connected to which of power supplies.

[0025] Figure 2 is an example of a circuit diagram of an LSI including a plurality of power supplies. A portion I shows a portion of the LSI to be actuated with a supply voltage VDD1, and a portion II shows a portion thereof to be actuated with a supply voltage VDD2. Table 2 is the net list A of the circuit diagram of Fig. 2 produced according to the first embodiment of the present invention.

[0026]

[Table 2]

Net List of Fig. 2									
G1	BI1N1	PAD	I3	Y	S1				
G3	V01S1	A	S1	Y	S2				
G2	BI1N1	PAD	I2	Y	S3				
G4	N02S1	A	S2	B	S3	Y	S4		
G5	BO1N1	A	S4	PAD	O2				
G6	BI1N2	PAD	I1	Y	S5				
G7	V01S2	A	S5	Y	S6				
G8	BO1N2	A	S6	PAD	O1				

[0027] Next, actions to be performed for development of a net

list in the CAD system in accordance with the first embodiment of the present invention will be described by taking for instance a case where the circuit diagram of Fig. 2 is converted into the net list of Table 2. In general, the property of a cell varies depending on whether the cell is actuated with a supply voltage VDD1 or a supply voltage VDD2, though the cell is one the same cell. Therefore, a cell to be driven with the supply potential VDD1 and a cell to be driven with the supply potential VDD2 are registered as different types of cells in the library A 20. For example, a cell 21 and a cell 22 share the same capability expressed as BI1N. However, since the cell 21 is included in the portion of the LSI that is associated with the portion I and driven with the supply voltage VDD1, the cell 21 has its name changed to BI1N1. The cell 22 is included in the portion of the LSI that is associated with the portion II and driven with the supply voltage VDD2, and has therefore its name changed to BI1N2. For this change, a user may be prompted to rename cells at the time of producing a circuit diagram. Otherwise, the CAD system may autonomously change names of cells in consideration of the portion to be driven with the voltage VDD1 and the portion to be driven with the voltage VDD2.

[0028] As mentioned above, the net list of Table 2 is produced by changing cell names. In the library A 20, cells BI1N1, BI1N2, V01S1, V01S2, N02S1, N02S2, B01N1, and B01N2 are registered.

[0029] Thereafter, the same processing as that performed in the conventional system is performed in order to produce mask data and a test program for an LSI in which a plurality of power supplies is used in combination. Namely, the thus created net list is used to first perform virtual wiring length-based logical simulation 15, whereby the logic of the LSI is verified. If the result of the logic verification 15a demonstrates that desired logic is not attained, a circuit diagram is reproduced and hierarchical development 14 is performed. If desired logic is attained, layout 16 is performed. After layout is completed, real wiring length-based logical simulation 17 is performed. Logic verification 17a is then performed. If desired logic is

not attained, layout is resumed or a circuit diagram is reproduced. If desired logic is attained, mask data 16a produced by the layout block 16 is used to create a mask. An LSI is then fabricated. Thereafter, a test program 18a is produced.

[0030] As mentioned above, according to the present embodiment, when a circuit diagram is developed into a net list, cell names are modified so that portions of the net list associated with portions of an LSI to be driven with different supply voltages can be distinguished from each other. This provides the advantage that a CAD system for LSIs including a plurality of power supplies can be realized.

[0031] The present embodiment is concerned with a case where two power supplies supply voltages VDD1 and VDD2 are used in combination. Even when two or more supply voltages are used in combination, the present invention can be implemented in the same manner.

[0032] (Second Embodiment) In the foregoing embodiment, cell names are modified in order to realize a CAD system for LSIs including a plurality of power supplies. Alternatively, signal names may be modified. In this case, not only the same advantage as that of the foregoing embodiment but also the merit that a storage capacity can be reduced is provided for a CAD system.

[0033] Figure 3 briefly describes the overall flow of actions to be performed in a CAD system in accordance with another embodiment of the present invention by taking a gate array CAD system for instance. In the drawing, reference numeral 21 denotes a hierarchical development block that flatly develops a circuit diagram having a hierarchical structure, and transmits a net list by providing internal components such as macro functions and simulation models in the form of a library. The hierarchical development block 21 has the capability to change the names of signals to be transferred from cells, which share the same capability and are driven with different supply potentials, according to the supply potentials. Reference

numeral 15 denotes a virtual wiring length-based logical simulation block that converts a virtual wiring length, which is registered in a library, into a resistive or capacitive component so as to calculate a delay, and performs simulation on the basis of the result of the calculation. Reference numeral 16 denotes a layout block that arranges circuit elements, which are indicated in a circuit diagram, in the form of an LSI, and routes signals among the circuit elements. Reference numeral 17 denotes a real wiring length-based logical simulation block that converts a real wiring length, which is determined as a result of layout, into a resistive or capacitive component so as to calculate a delay, and performs simulation on the basis of the result of the calculation. Reference numeral 18 denotes a test program production block that uses a test pattern, which the logical simulation blocks 15 and 17 use for simulation, to produce a test pattern based on which a product is checked to see if it is acceptable or defective. Reference numeral 22 denotes a net list B produced by the hierarchical development block 21 according to the present embodiment. Reference numeral 23 denotes a library required by the CAD system in accordance with the present embodiment. The library 23 includes a library B 23a and a library C 23b.

[0034] The hierarchical development block 21, logical simulation block 15, layout block 16, logical simulation block 17, test program production block 18, and libraries 23a and 23b that are shown in Fig. 3 have fundamentally the same capabilities as the hierarchical development block 14, logical simulation block 15, layout block 16, logical simulation block 17, test program production block 18, and library 20 respectively that are shown in Fig. 1. However, in the CAD system shown in Fig. 3, the libraries B and C that are normal libraries associated with a sole power supply can be used as they are to simulate an LSI including a plurality of power supplies.

[0035] Figure 4 shows an example of a circuit diagram of an LSI including a plurality of power supplies. A portion I shows

a portion of the LSI to be actuated with a supply voltage VDD1, and a portion II shows a portion thereof to be actuated with a supply voltage VDD2. Table 3 is a net list B of the circuit diagram of Fig. 4 which is produced according to the second embodiment of the present invention.

[0036]

[Table 3]

Net List of Fig. 4						
G1	BI1N	PAD	I3	Y	S1A	
G3	V01S	A	S1A	Y	S2A	
G2	BI1N	PAD	I2	Y	S3A	
G4	N02S	A	S2A	B	S3A	Y S4A
G5	BO1N	A	S4A	PAD	O2	
G6	BI1N	PAD	I1	Y	S5B	
G7	V01S	A	S5B	Y	S6B	
G8	BO1N	A	S6B	PAD	O1	

[0037] Next, actions to be performed for development of a net list in the CAD system in accordance with the second embodiment of the present invention will be described by taking for instance a case where the circuit diagram of Fig. 4 is converted into the net list of Table 3. Signals 24, 26, 28 and 30 are initially stated in a net list as I1, S5, S6, and O1 respectively. The input signal I1 is an input signal transferred to the portion of the LSI to be driven with the supply voltage VDD2. The output signal 26 of a cell 25 is temporarily renamed to S5B by appending a suffix letter B to S5. Likewise, the output signal 28 of a cell 27 to which the signal whose name has the suffix letter B appended thereto is renamed to S6B by appending the suffix letter B to S6. This processing is repeatedly performed.

[0038] According to the present invention, the names of external pins include no suffix letter. A suffix letter A is appended to names of signals to be transferred within the portion to be driven with the supply voltage VDD1. Thus, cell names are changed, and the net list B of Table 3 is completed.

[0039] Information on cells to be driven with the supply potential VDD1, such as, BI1N, VO1S, and BO1N is put in the

library B 23a. Information on cells to be driven with the supply voltage VDD2, such as, BI1N, V01S, N02S, and B01N is put in the library C 23b. Which of the libraries should be referenced depends on the suffix letter. Namely, if the name of an output signal of a cell includes the suffix letter A, the library B should be referenced. If the name thereof includes the suffix B, the library C should be referenced.

[0040] Hereinafter, the same processing as that performed in the conventional system and the system shown in Fig. 1 alike is performed. Eventually, intended mask data and an intended test program are produced. In short, the net list produced as mentioned above is used to first perform virtual wiring length-based logical simulation 15. Thus, the logic of an LSI is verified. If the result of the logic verification 15a demonstrates that desired logic is not attained, a circuit diagram is reproduced and hierarchical development 21 is performed. If desired logic is attained, layout 16 is performed. After the layout is completed, real wiring length-based logical simulation 17 is performed. Logic verification 17a is then performed. If desired logic is not attained, layout is resumed or a circuit diagram is reproduced. If desired logic is attained, mask data 16a produced by the layout block 16 is used to create a mask. An LSI is then fabricated. Thereafter, a test program 18a is produced.

[0041] As mentioned above, according to the present embodiment, cell names are not modified but signal names are modified in order to realize a CAD system for LSIs including a plurality of power supplies. Consequently, in addition to the same advantage as that of the first embodiment that an LSI including a plurality of supply voltages can be designed, an advantage described below is provided. Namely, according to the first embodiment, although circuit elements share the same capability, since supply voltages with which the circuit elements are driven are different from one another, three libraries associated with 3 V, 5 V, and the combinational use of 3 V and 5 V are needed. According to the second embodiment, the library A for the

combinational use of a plurality of power supplies needed in the first embodiment may not be prepared but the normal libraries B and C each associated with a sole power supply can be used as libraries associated with the combinational use of a plurality of power supplies as they are. This leads to a reduced storage capacity and an improved response speed.

[0042] The present embodiment is concerned with a case where two supply voltages are used in combination. Alternatively, the present invention can be implemented in a case where two or more supply voltages are used in combination.

[0043] Moreover, the above embodiments have been described by taking a gate array CAD system for instance. The present invention may be adapted to a CAD system for designing an application-specific IC (ASIC) or the like. Even in this case, the present invention provides the same advantages as those of the embodiments.

[0044]

[Advantages] As mentioned above, according to a semiconductor design supporting system in which the present invention is implemented, when a circuit diagram is developed into a net list, names of cells that share the same capability and are driven with different supply potentials are changed according to the supply potentials. Thus, portions of the net list associated with portions of an LSI to be driven with different supply voltages can be distinguished from each other. A CAD system capable of designing an LSI including a plurality of power supplies can be provided.

[0045] Moreover, according to a semiconductor design supporting system in which the present invention is implemented, when a circuit diagram is developed into a net list, names of signals transferred from cells that share the same capability and are driven with different supply potentials are changed according to the supply potentials. Consequently, portions of the net list associated with portions of an LSI to be driven with different supply voltages can be distinguished from each other. This obviates a library associated with the

combinational use of a plurality of power supplies. Thus, a CAD system capable of designing an LSI, which includes a plurality of power supplies, despite a limited storage capacity can be provided.

[Brief Description of the Drawings]

[Fig. 1] Figure 1 briefly describes the overall flow of actions to be performed in a semiconductor design supporting system in accordance with an embodiment of the present invention.

[Fig. 2] Figure 2 is a circuit diagram of an LSI including a plurality of power supplies.

[Fig. 3] Figure 3 briefly describes the overall flow of actions to be performed in a semiconductor design support system in accordance with another embodiment of the present invention.

[Fig. 4] Figure 4 is a circuit diagram of an LSI including a plurality of power supplies.

[Fig. 5] Figure 5 schematically shows the overall configuration of semiconductor design support systems in accordance with a related art and the embodiments of the present invention.

[Fig. 6] Figure 6 briefly describes the overall flow of actions to be performed in a conventional CAD system.

[Fig. 7] Figure 7 is a circuit diagram that has not been hierarchically developed.

[Description of Reference Numerals]

14, 21: hierarchical development block

15: virtual wiring length-based logical simulation block

16: layout block

17: real wiring length-based logical simulation block

18: test program production block

19, 22: net list

20, 23: library

<DRAWINGS>

Fig. 1

14a: CIRCUIT DIAGRAM

14: HIERARCHICAL DEVELOPMENT

19: NET LIST A

15: VIRTUAL WIRING LENGTH-BASED LOGICAL SIMULATION

15a: VERIFICATION

16: LAYOUT

17: REAL WIRING LENGTH-BASED LOGICAL SIMULATION

17a: VERIFICATION

18: TEST PROGRAM PRODUCTION

20: LIBRARY A

16a: MASK DATA

18a: TEST PROGRAM

Fig. 3

CIRCUIT DIAGRAM

21: HIERARCHICAL DEVELOPMENT

22: NET LIST B

15: VIRTUAL WIRING LENGTH-BASED LOGICAL SIMULATION

15a: VERIFICATION

16: LAYOUT

17: REAL WIRING LENGTH-BASED LOGICAL SIMULATION

17a: VERIFICATION

18: TEST PROGRAM PRODUCTION

23a: LIBRARY B

23b: LIBRARY C

16a: MASK DATA

18a: TEST PROGRAM

Fig. 5

103: DISPLAY DEVICE

102: DISK DRIVE

104: KEYBOARDING INPUT DEVICE

101: STORAGE DEVICE